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10/536,732	05/27/2005	Eric Desmicht	348162-982430	4315

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EXAMINER	
OKEKE, IZUNNA	

ART UNIT	PAPER NUMBER
2432	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/536,732	DESMICHT ET AL.	
	Examiner	Art Unit	
	IZUNNA OKEKE	2432	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 5-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 5-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/16/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments have been fully considered but they are not persuasive.

With respect to amended claim 1, applicant argues on page 7 of the arguments/remarks that Sakaki fails to anticipate the amended claim. Amended claim 1 now recites the limitation "wherein said protection data is only modifiable so as to increase said protection level by permanently reducing access to a part of the protected data memory portion". The specification does not define or disclose the phrase "permanently reducing access" but instead discloses, "when the protection is modified to increase the protection data, access to the protected data or memory storing the protected data is refused" (See Para 34). Examiner has reviewed the portions of the specification quoted by applicant in support of the amendment but found no support for the phrase "permanently reducing access to a part of the protected memory". However, Para 34 more clearly defines the process of modifying protection data so as to increase the protection level by refusing access to the protected data. Sakaki discloses this limitation with the use of the s1, s2 protection bits. As quoted in Col 5, Line 13-62, Sakaki discloses a method of protecting a test program that is stored in the memory of a chip using the security bits s1, s2. Before shipment (during manufacture) the bits are in the low state and the test program can be executed (Col 5, Line 24-33). After memory test (at the manufacturer), the s1 bit is brought to the high level while the s2 bit remain at the low level and the chip is shipped with the protection bits in that state (Col 5, Line 43-47). After shipment, when the chip is turned on, the s2 bit goes to the high state (modified protection data to increase the level of protection) and access to test program (protected data) is denied/refused/reduced (Col 5, Line 49-62).

With respect to claim 7, Sakaki discloses restricting access to the address range where the protected test program is stored when the s1, s2 protection bit are set (Col 6, Line 5-14). The test program is stored in an address range in memory and other programs that can be accessed are also stored in other address ranges. When the protection bits are set (which disables access to the protected address range), access to the address range storing the protected test program is made impossible.

The argument with respect to the 103 rejection hinges on amended claim 1 which has been addressed above.

Claim Objections

2. Claim 17 is objected to because of the following informalities: Claim 17 cannot depend on itself. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1, 9, 11, 15-17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The cited claims recites the limitation "wherein said protection data is only modifiable so as to increase said protection level by permanently reducing access to a part of the protected data memory portion". There is no disclosure in the specification supporting this

limitation or the phrase "permanently reducing access". The full scope and meaning of the phrase "permanently reducing access" cannot be determined from the specification. By "reducing access", is the limitation directed to completely denying access? Partially denying access? granting access but on a reduced level? The disclosure in the specification is "refusing/denying access to the protected data" and this disclosure does not support the newly added limitation.

Claim Rejections - 35 USC § 102

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1, 3, 5, 7-8, 9, and 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakaki et al. (US-5826007).

a. *Referring to claim 1, 9 and 11:*

Regarding claim 1, Sakaki teaches a chip comprising a microprocessor, and an integrated non-volatile programmable memory that stores protection data in a protection data memory portion and protected data in a protected data memory portion (Col 4, Line 13-48…… chip comprising CPU, NV-RAM storing protected test memory (storing a test program) and protection bits (S1, S2) for protecting access to the protected memory), wherein said protection data defines a protection level for authorizing[[/]] or denying access to said protected data memory portion by said microprocessor while a program is executed (Col 4, Line 42 thru Col 5, Line 48…. The protection bits (s1, S2) define a protection level for the protected data in that access (Read/write) to the data is authorized when the bits are in their low level (logic 0) and denied when s1 is changed to a high level (logic 1)), and wherein said protection data is only

modifiable so as to increase said protection level by permanently reducing access to a part of the protected data memory portion (See the response to argument, Col 5, Line 13-62.... protection bit s2 is modified to high level (logic 1) after shipment to increase the protection level from the initial state and deny access to the stored test program)and said protected data includes data to activate[[/]] or deactivate an optional feature of the chip (Col 4, Line 28-30 and Col 5, Line 34-42.... protected test program used to enable/disable read/write (input/output) to the NV memory from an external terminal).

a. *Referring to claim 3:*

Regarding claim 3, Sakaki teaches a chip according to Claim 1, wherein said protection data includes a password, said access being authorized/denied through a password check (Col 5, Line 13 thru Col 6, Line 12..... s1 and s2 protection bits with s2 comprising the password check. If s1=1, the chip is password-protected and access to the protected data is denied. If s1=1 and s2=1 (s2 being the password check), a manufacturer can then access the protected data after shipment).

a. *Referring to claim 5:*

Regarding claim 5, Sakaki teaches a chip according to Claim 1, wherein said optional feature is a connection to an external device for downloading a program and/or data from said external device (Col 5, Line 34-43.... connection to an external terminal for inputting or outputting data into the memory of the chip).

a. *Referring to claim 7:*

Regarding claim 7, Sakaki teaches a chip according to Claim 1, wherein said protection data includes at least one address value defining an address limit from which the data stored at

said memory are protected data and access to such protected data is denied (See the response to argument and Col 6, Line 3-16 and Col 6, Line 5-14.... based on the value of the s1, s2 protection bits, the bus control logic defines the address of the protected data (test program) which the CPU can execute).

a. *Referring to claim 8:*

Regarding claim 8, Sakaki teaches a chip according to Claim 7, wherein said protected data include includes programs and data operating a conditional-access dedicated microprocessor (Col 4, Line 13-35.... protected memory storing system program and fixed data for operating a microprocessor) .

a. *Referring to claim 12:*

Regarding claim 12, Sakaki teaches a chip according to Claim 1 further comprising a random logic coupled between said integrated non-volatile programmable memory and a connection bus of said microprocessor (Fig 2. bus line control circuit coupled between the protected memory and the processor).

Claim Rejections - 35 USC § 103

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. Claim 6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakaki et al. (US-5826007), and further in view of Madter et al. (US-20050033951).

a. *Referring to claim 6:*

Regarding claim 6, Sakaki teaches the protected data includes data to activate/deactivate and external feature of the microprocessor such as write/read to an external terminal. Sakaki does

not teach external feature of downloading a boot program from an external memory. However, the concept of protecting a chip from downloading an external boot program (which might be malicious) using protection bits is well known in the art. For instance, Madter discloses an on-chip security method wherein a security value (protection data) is used to protect flash memory. The password is used to protect access to instructions for downloading an external boot program to be run by the chip. When a password is received (password check), download of the external boot program is inhibited (See Sakaki, Para 32-35). Therefore, it would have been obvious to modify Sakaki's protection system to include protection against downloaded boot programs wherein the protection bits of Sakaki are used to enable or disable access to external boot programs for the purpose of securing the chip from both unauthorized and malicious access.

a. *Referring to claim 10:*

Regarding claim 10, Sakaki teaches a device as claimed in Claim 9, wherein the device is intended to process encrypted video/audio data (See Madter, Para 3… PDA and mobile devices for processing encrypted video/audio as known in the art).

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakaki et al. (US-5826007) and Madter et al. (US-20050033951), and further in view of Boyle et al. (US-6118870).

a. *Referring to claim 13:*

Regarding claim 13, Sakaki teaches a chip according to claim 1. Sakaki does not explicitly teach the chip having a MIPS instruction set. However, Boyle teaches a chip having a MIPS instruction set (See Boyle, Col 10, Line 3-18). Therefore it would have been obvious to one of ordinary skill to implement Sakaki's chip as a microprocessor having a MIPS instruction

set for the benefit of utilizing RISC architecture which provides higher performance by making instruction execute quickly and is designed for use with high level programming languages.

10. Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakaki et al. (US-5826007) and Madter et al. (US-20050033951), and further in view of Moller et al. (US-20030014653).

a. *Referring to claim 14:*

Regarding claim 14, Sakaki teaches the method of claim 11 wherein the protected data is a test program defined by an address range which is protected by protection data (bits) which is modifiable to increase the protection by denying access to the test program. Sakaki does not teach the chip protecting a stored conditional access program (such as encryption/decryption program for content) using the mechanism for protecting the test program. However, storing and protecting conditional access programs (such as encryption/decryption program for content) on a chip is well known in the art. For instance, Moller discloses a method of storing a conditional access programs (such as encryption/decryption program for content) on a chip and protecting access to the program using protection bits (See Moller, Para 6-8). Therefore, one of ordinary skill would have been motivated to modify Sakaki's teaching to store a conditional access program on the chip and to protect access to the program using the same mechanism used to protect the test program. This is advantageous in the art of media and content distribution wherein the decryption key program is stored on the chip of an STB or media player and protected from unauthorized users using the protection bits (i.e if a correct password is not received, the protection bits are modified to restrict access to the decryption program).

a. *Referring to claim 15:*

Regarding claim 15, the combination of Sakaki, Madter and Moller teaches the method of claim 14 wherein the access to the part of the first protected data memory portion is permanently reduced by modification of the first set of address data (See the rejection in claims 7 and 14).

a. *Referring to claim 16:*

Regarding claim 17, the combination of Sakaki, Madter and Moller teaches the method of claim 15 further comprising: using at least a second authorized access to modify a second protected data portion in the first integrated non-volatile memory, wherein the second protected data portion comprises a set of conditional access microprocessor data and a deciphering key, with the deciphering key allocated to a lowest address of the second protected data portion; protecting the access to the second protected data portion in the first integrated non-volatile memory by modifying a second protection data portion of the first integrated non-volatile memory in order to deny access to the second protected data portion, wherein said second protection data portion is only modifiable so as to increase said protection level by permanently reducing access to at least a part of the second protected data memory portion (See the rejection in claims 1, 14 and 15).

a. *Referring to claim 17:*

Regarding claim 17, the combination of Sakaki, Madter and Moller teaches the method of claim 17 wherein the second protection data portion comprises a second address data that is the lowest address in the second protected data portion readable by the microprocessor, wherein the set of address data is initially associated with the lowest address of the second protected data portion; and wherein the second protection data portion is only modifiable so as to increase said

protection level by increasing the value of the second address data (See the rejections in claims 1, 14 and 15).

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to IZUNNA OKEKE whose telephone number is (571)270-3854. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on (571) 272-3799.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/IZUNNA OKEKE/
Examiner, Art Unit 2432

/Gilberto Barron Jr./
Supervisory Patent Examiner, Art Unit 2432